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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,195	03/01/2005	David A. Fish	GB 020146	6444

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EXAMINER	
ABDIN, SHAHEDA A	
ART UNIT	**PAPER NUMBER**
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,195	FISH ET AL.	
	Examiner	Art Unit	
	Shaheda A. Abdin	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 9-14, 16- 17,* is/are rejected.

7)☒ Claim(s) *5-8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 3-13-06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Abstract

4. This application does not contain an abstract of the disclosure as required by 37 CFR 1.72(b). An abstract on a separate sheet is required.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 13, 14, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Shannon et al. (WO 01/20591 A1, see the IDS).

(1) Regarding claim13:

Shannon teaches (in Fig. 3) a method of driving an active matrix electroluminescent display device comprising an array of display pixels (10) each comprising a drive transistor (22) and an electroluminescent display element (20), the method comprising, for each addressing of the pixel:

applying a drive voltage (i.e. VA) to an input of the pixel (i.e. 10);

modifying the drive voltage (VA) by an amount corresponding to the threshold voltage of the drive transistor (22) (page 12, lines 15-32, and page 13, lines 21-30);

storing the modified drive voltage in a capacitor (i.e. 36) arrangement and applying the modified drive voltage to the gate of the drive transistor (i.e. 22) , thereby compensating for threshold variations between drive transistors of different pixels (page13, lines 21-29, page 17,lines 1-18);

discharging the capacitor (i.e. 36) arrangement using a photodiode (i.e. 38) illuminated by the light output of the electroluminescent display element (i.e. 20), thereby compensating for aging variations between pixels (page 12, lines 16-32, and Fig. 3).

(2) Regarding claim 14:

Shannon teaches wherein storing the modified drive voltage (i.e. changed voltage) comprises storing the modified drive voltage on a capacitor (i.e. 36) (page13, lines 21-29, page 17,lines 1-18);

(3) Regarding claim 16:

Shannon teaches storing the modified drive voltage comprises pumping the drive voltage (i.e. increasing the voltage level) onto a storage capacitor (i.e. 36) on which a voltage corresponding to the threshold voltage was previously provided (i.e. predetermined voltage) (page 17, lines 1-18).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-4, 9-12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shannon (WO 01/20591 A1) Fig. 3, in view of Shannon (WO 01/ 20591 A1), Fig. 8.

(1) Regarding claim 1:

Shannon teaches (in Fig. 3) an active matrix electroluminescent display device comprising an array of display pixels (i.e. 10), each pixel comprising:

an electroluminescent display element (i.e. i.e. 20) (page 12, lines 15-32) ;

a drive transistor (i.e. 22) for driving a current through the display element (i.e. 20) (page 12, lines 15-32);

a storage capacitor (36) for storing a voltage to be used for addressing the drive transistor (i.e. 22) (page 12, lines 15-32, and page 13, lines 1-11) ;

a discharge photodiode (38) for discharging the storage capacitor (36) in dependence on the light output of the display element (page 12, lines 15-32);

a circuit element (i.e. 26) for changing an input data voltage (VA) applied to the pixel (20) by an amount corresponding to the threshold voltage of the drive transistor

(page 12, lines 15-32, and page 13, lines 21-30), and for applying the changed data voltage (i.e. gradual voltage changed at the gate node 24) between the gate and source of the drive transistor (22) (note that photodiode 38 is connected to storage capacitor and arranges to be reverse biased in the drive period so as to leak charge from the storage capacitance in response to light from the display element falling thereon at a rate depends on the level of the incident light in the drive period and a gradual voltage changed occurred at the node 24 which is achieved by desired gray scale level, see column 9, lines 1-7).

Note that above Shannon does not teach circuit elements for changing an input data voltage applied to the pixel.

However, the limitation "circuit elements" does not define a patentably distinct invention over "Shannon" since the invention as a whole and Shannon (In Fig. 8) are directed to changing an input data voltage applied to the pixel (i.e. 10) by using circuit elements (26, 50, 51)(see the illustration in Fig. 8, page 21, lines 25-32, and page 22, lines 1-8).

Therefore, it would have been obvious to a person of ordinary skill in the art to utilize circuit elements (such as 26, 50, 51) for changing an input data voltage applied to the pixel (20) by an amount corresponding to the threshold voltage of the drive transistor, and could be applying the changed data voltage between the gate and source of the drive transistor (22). In this configuration the system would provide

uniformity in the display out put by avoiding unwanted variation in the display element currents.

(2) Regarding claim 2;

Shannon teaches wherein each pixel (i.e. 10) further comprises an address transistor (i.e. 26) connected between a data signal line (14) and an input to the pixel (e.g. in put to the element 2) (see the illustration in Fig. 3).

(3) Regarding claim 3:

Shannon teaches the drive transistor (i.e. 22) is connected between a power supply line (30) and the display element (20) page 12, lines 15-32.

(4) regarding claim 4

Shannon teaches storage capacitor (i.e. 36) is connected between the power supply line (30) and the gate of the drive transistor (22).

(5) Regarding claim 9:

Shannon teaches the storage capacitor (36) and the discharge photodiode (38) are connected in parallel between the power supply line (30) and an input to the pixel (see the illustration in Fig. 3),

Note that in Fig. 5, Shannon teaches the circuit elements comprise a threshold storage capacitor (i.e. 36) connected between the input and the gate of the drive transistor (22) (page 15, lines 5-16).

(6) Regarding claim 10:

Shannon teaches the circuit elements further comprise a bypass transistor (i.e. 40) connected between the source and gate of the drive transistor (22) for charging the threshold storage capacitor (36) to the threshold voltage using a current of the drive transistor (22) (page 16, lines 14-29 and page 17, lines 1-18) .

(7) Regarding claim 11:

Shannon teaches (in Fig. 3) an active matrix electroluminescent display device comprising an array of display pixels (10), each pixel comprising:

an electroluminescent display element (i.e. 20)

and a photodiode (i.e. 38) for discharging the storage capacitor (i.e. 36) in dependence on the light output of the display element.

Note that Shannon (In Fig. 8) teaches a current sampling (i.e. 50, Fig. 8) circuit for sampling a drive current and including a drive transistor (22) for driving current through the display element (i.e. 20) (page 21, lines 25-32, page 22, lines 1-8, and Fig. 8);

a storage capacitor (i.e. 36) for storing a gate-source voltage for the drive transistor (22) corresponding to the sampled drive current (page 21, lines 25-32, page 22, lines 1-8, and Fig. 8). Thus the reference of Shannon teach the claim limitations.

(8) Regarding claim 12:

Shannon teaches the current sampling circuit (i.e. 50) comprises an isolating transistor (i.e. 40) for selectively isolating the drive transistor (22) from the display element (20) and a bypass transistor (i.e. 51) for selectively connecting the drive transistor (22) to the input of the pixel (page 21, lines 25-32, page 22, lines 1-15, and Fig. 8).

(9) Regarding claim 17.

Note that the limitations of claim 17 are analyzed same as claim 11 above, see the discussion in claim 11.

Allowable Subject Matter

9. Claims 5-8 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is an examiner's statement of reasons for allowance:

(1) Regarding claim 8:

The closest prior art of record does not teach or suggest a second photodiode and a second storage capacitor, wherein the second photodiode is connected between the gate of the drive transistor and one terminal of the second storage capacitor.

(2) Regarding claim 8:

The closest prior art of record Stewart (US Patent No: 5952789) teaches circuit elements (T7 and T6, Fig. 4) which are comprised two oppositely facing transistors (50,52) but does not teach or suggest the circuit elements (T7 and T6) comprises two

parallel oppositely facing diode-connected transistors, connected between the input to the pixel and the gate of the drive transistor.

(3) Regarding claim 15:

The closest prior art of record Stewart (US Patent No: 5952789) teaches second capacitor (e.g. 0.5c2, Fig. 4), but Stewart does not teach storing a voltage corresponding to the threshold voltage of the drive transistor on a second capacitor.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's discloser.

Kimura (US 6529178 B1) discloses a current driven emissive display device, method for driving the same, and method for manufacturing the same.

Inquiry

12. Any inquiry concerning this communication should be directed to the examiner, Shaheda Abdin, at (571) 270-1673 Monday- Friday 7:30 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached at (571) 272-7691.

Information regarding the status on an application may be obtained from the Patent Application information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (tool-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9799 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of patents and trademarks

Washington, D.C. 20231

Or fax to:

(703)872-9314 (for Technology Center 2600 only)

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02/14/2008

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